Amendments to the Claims :

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-17(canceled)

18.(new) A differential Ternary content addressable memory (TCAM) cell comprising:

two storage memory cells;

two pair N transistors connected to match line; and

two pair N transistors connected to dummy line.

19(new). The differential TCAM cell of claim 18, wherein the two memory cells store the corresponding value encoded from data bit and mask bit respectively, the contents stored in the two memory cell are called X bit and Y bit.

20(new). The differential TCAM cell of claim 18, wherein the two pair N transistor connected to match line logically work as a comparator to compare the input data and its complementary with X bit and Y bit stored in the two memory cells.

21(new). The differential TCAM cell of claim 18 , wherein the capacitance loading to dummy line of two pair N transistor connected to dummy line are equal to the capacitance loading to match line of the two pair N transistor connected to match line.

22(new). The differential TCAM cell of claim 18, wherein the two pair N transistors

connected to dummy line are logically OFF and

conduct no current from dummy line to GND.

23(new) . A ternary content addressable memory array comprising:

a plurality column of differential TCAM cells and a plurality row of differential TCAM cells ;

a column dummy differential content addressable cells connected to

the corresponding row;

a column differential sense amplifiers connected to the corresponding row; and

a pair column current sources connected to match line and dummy line in each corresponding row.

24 (new) A ternary content addressable memory array of claim 23, wherein the dummy cell have a pair N transistor connected to match line and a pair N transistor connected to dummy line.

25(new). A ternary content addressable memory array of claim 23, wherein the pair N transistor connected to dummy line conduct less current than the pair N transistor connected to match line of differential Ternary content addressable memory (TCAM) cell of claim 18.

26(new). A ternary content addressable memory array of claim 23, wherein the pair N transistor connected to match line are OFF.

27(new). A ternary content addressable memory array of claim 23, wherein the dummy line and match line are pre-charged to low voltage level close or equal to GND before comparison.

28.(new) A ternary content addressable memory array of claim 23, wherein a pair column current sources connected to match line and dummy line in each corresponding row conduct current to dummy line and match line, and pull up the electrical potential of the dummy line and the electrical potential of match line from the pre-charged low voltage level.

29(new). A ternary content addressable memory array of claim 23, wherein a pair column current sources are a pair column P transistors connected to Vdd.

30(new) A ternary content addressable memory array of claim 23, wherein differential each sense amplifier connected to the corresponding row detect Hit or miss based on the voltage difference between match line and dummy line of claim 28.

31(new) A method for detecting a Hit or a MISS in a content addressable memory(CAM), comprising the steps of :

pre-charging the match line and dummy line to low voltage level close or equal to ground voltage level;

pulling up the voltage level of match line and dummy line through current sources; and sampling the voltage difference between match line and

dummy line to determine Hit or Miss.

32(new). A method for detecting a Hit or a MISS in a content addressable memory of claim 31, wherein the sampling time are determined by a timing circuit.

33(new). A method for detecting a Hit or a MISS in a content addressable memory of claim 32, wherein the timing circuit is similar to a row of the CAM.